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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,734	10/02/2000	Einar Hansson	1	3417

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AGERE SYSTEMS INC.
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EXAMINER	
KUMAR, PANKAJ	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,734	HANSSON, EINAR	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,8-14 and 16-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5, 8-12, 16-17* is/are allowed.

6)☒ Claim(s) *13,18-22 and 24-28* is/are rejected.

7)☒ Claim(s) *14 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments are moot in view of the new grounds of rejection. Although some claims have previously indicated allowable subject matter added, those subject matter are not allowable based on some of amendments as certain limitations from the prior independent claims have been removed.

Response to Amendment

Claim Rejections - 35 USC § 103

2. Claims 6, 7, 15 have been cancelled.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13, 18-22, 24-26, 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cotton 5,870,441. Here is how the reference teaches the claims:

5. As per claim 13: A method for clock and data recovery comprising the steps of: receiving a data signal of a first frequency (Cotton fig. 4d-2: input into 150; fig. 6: link data), defining a timing signal (Cotton fig. 4d-1, 4d-2: output from VCXO 100 and into 148) of a second frequency (Cotton does not teach a second frequency but would be obvious as explained below), dividing a cycle of the timing signal into a number of N clock phases (Cotton fig. 5a; fig. 6: phase 0-3; fig. 4d-2: divide by 2 in 148), sampling a portion of said data signal by a data

sampling component (Cotton fig. 4d-2: 150 is sampling input into 150 at the 4 phases) resulting in a binary number (Cotton fig. 8b), said data sampling component comprising a buffer component buffering said data signal (Cotton fig. 9: D-flip-flops buffer at D input) and comprising a phase detector (Cotton fig. 9: D-flip-flops are detecting phase at their clock input), looking up said binary number in a truth table yielding a logic output statement (Cotton fig. 7: right side of table has binary numbers; fig. 8b, 10a, 10b have outputs based on binary number inputs), and transmitting said logic output statement to a phase selector wherein the data signal is a binary signal having signal states zero or one defining a bit sequence and wherein said data signal is buffered by a first, a second and a third group of bistable multivibrators (Cotton fig. 6: flip-flops are buffering), triggered by a first clock phase i, a second clock phase j and a third clock phase k, respectively, resulting in a buffering of the state of said data signal at said clock phases i, j, and k (Cotton fig. 6: flip-flops are buffering and are triggered by different clock phases).

6. What Cotton does not teach is that the timing signal is of a second frequency. It is common knowledge, based on the Nyquist criteria, that the sampling signal has to be at least twice as fast as the data signal in order to avoid aliasing. Thus, it would have been obvious to one skilled in the art at the time of the invention to modify Cotton to arrive at the timing signal of a second frequency as recited by the instant claims, because Cotton suggests sampling correctly, and this means that aliasing should be avoided by having a sample timing be at least twice the data rate, in the analogous art of data sampling.

7. As per claim 18: a method for clock and data recovery further comprising the steps of: receiving a data signal of a first frequency (Cotton fig. 4d-2: input into 150; fig. 6: link data); defining a timing signal (Cotton fig. 4d-1, 4d-2: output from VCXO 100 and into 148) of a second frequency (Cotton does not teach a second frequency but would be obvious as explained below); dividing a cycle of the timing signal into a number of N clock phases (Cotton fig. 5a; fig. 6: phase 0-3; fig. 4d-2: divide by 2 in 148); sampling a portion of said data signal by a data sampling component (Cotton fig. 4d-2: 150 is sampling input into 150 at the 4 phases) comprising a buffer component buffering said data signal (Cotton fig. 9: D-flip-flops buffer at D input) and comprising a phase detector (Cotton fig. 9: D-flip-flops are detecting phase at their clock input), said step of sampling further including detecting the state of the data signal at a clock phase i of the previous cycle of the timing signal (Cotton col. 18 lines 32-37: ""Flip-Flop Values" of 1100 or 0011 where there are an equal number of ones and zeros require special consideration when determining what binary value to assign to the incoming bit. In such cases, the previous history of the samples must be known in order to assign a value to the sampled pattern."), resulting in a four digit binary number having sixteen possible values (Cotton fig. 7: right side of table has 4 digit binary numbers which result in 16 possible values); looking up said four digit binary number in a truth table yielding a logic output statement (Cotton fig. 7: 16 cases of phase alignments and 4 digit binary number associated with each one; fig. 8b, 10a, 10b; alternatively even if this teaching is not sufficient to teach the material limitations of the instant claims, a discussion is below); and transmitting said logic output statement to a phase selector (Cotton fig. 6: the data output of 176 is based on a phase and hence the phase is selected when the data is selected).

8. What Cotton does not teach is that the timing signal is of a second frequency. It is common knowledge, based on the Nyquist criteria, that the sampling signal has to be at least twice as fast as the data signal in order to avoid aliasing. Thus, it would have been obvious to one skilled in the art at the time of the invention to modify Cotton to arrive at the timing signal of a second frequency as recited by the instant claims, because Cotton suggests sampling correctly, and this means that aliasing should be avoided by having a sample timing be at least twice the data rate, in the analogous art of data sampling.

9. Cotton teaches looking up said four digit binary number in a truth table yielding a logic output statement (Cotton fig. 7: 16 cases of phase alignments and 4 digit binary number associated with each one; fig. 8b, 10a, 10b). Alternatively even if this teaching is not sufficient to teach the material limitations of the instant claims, Cotton teaches at least four possible phases, phases 0 to 3 in fig. 7, which could be represented by a two digit binary number. It is common knowledge to have different number of phases. Thus, it would have been obvious to one skilled in the art at the time of the invention to arrive at the four digit binary number for sixteen possible phases because Cotton suggests having multiple phases and representing with binary digits.

10. As per claim 19: A clock and data recovery circuit comprising: a first data input receiving a data signal of a first frequency (Cotton fig. 4d-2: input into 150; fig. 6: link data), a clock defining a timing signal (Cotton fig. 4d-1, 4d-2: output from VCXO 100 and into 148) of a second frequency (Cotton does not teach a second frequency but would be obvious as explained below), a phase generator dividing a cycle of the timing signal into a number of N clock phases

(Cotton fig. 5a; fig. 6: phase 0-3; fig. 4d-2: divide by 2 in 148); a data sampling component sampling a portion of said data signal (Cotton fig. 4d-2: 150 is sampling input into 150 at the 4 phases) causing a logic output statement based on a truth table (Cotton fig. 8b), said data sampling component comprising a buffer component for buffering said data signal (Cotton fig. 9: D-flip-flops buffer at D input) and comprising a phase detector coupled to said buffer component (Cotton fig. 9: D-flip-flops are detecting phase at their clock input), wherein the phase detector further detects the signal state of the data signal at a clock phase i (Cotton col. 18 lines 24-30) of the previous cycle of the timing signal (Cotton col. 18 lines 32-37: ""Flip-Flop Values" of 1100 or 0011) where there are an equal number of ones and zeros require special consideration when determining what binary value to assign to the incoming bit. In such cases, the previous history of the samples must be known in order to assign a value to the sampled pattern."), and a phase selector coupled to said data sampling component (Cotton fig. 6: the data output of 176 is based on a phase and hence the phase is selected when the data is selected).

11. What Cotton does not teach is that the timing signal is of a second frequency. It is common knowledge, based on the Nyquist criteria, that the sampling signal has to be at least twice as fast as the data signal in order to avoid aliasing. Thus, it would have been obvious to one skilled in the art at the time of the invention to modify Cotton to arrive at the timing signal of a second frequency as recited by the instant claims, because Cotton suggests sampling correctly, and this means that aliasing should be avoided by having a sample timing be at least twice the data rate, in the analogous art of data sampling.

12. As per claim 20: A clock and data recovery circuit as claimed in claim 19, further comprising: a counter (Cotton fig. 4d-2: 160) coupled between said data sampling component and said phase selector, wherein said logic output statement of said data sampling component causes said counter to count up, count down or hold.

13. As per claim 21: A clock and data recovery circuit as claimed in claim 19, wherein the data signal is a binary signal having signal states zero or one defining a bit sequence (Cotton fig. 7 right column).

14. As per claim 22: A clock and data recovery circuit as claimed in claim 19, wherein said buffer component comprises bistable multivibrators (Cotton fig. 6: flip-flops).

15. As per claim 24: A clock and data recovery circuit as claimed in claim 19, further comprising a first output receiving the data signal from the buffer portion which is triggered by the clock phase i (Cotton fig. 6: 176, 158, 166), wherein at least one of said data signal and said timing signal is transmitted by said first output (Cotton fig. 6: output of 176).

16. As per claim 25: A clock and data recovery circuit as claimed in claim 23, wherein the signal states of the data signal at the data outputs of said first, second and third buffer portions are detected by said phase detector (Cotton fig. 9: D-flip-flops are detecting phase at their clock input at the multiple flip-flops which provide buffering).

17. As per claim 26: A clock and data recovery circuit as claimed in claim 19, further comprising a low pass filter coupled to said phase detector (Cotton fig. 4d-1: 102; col. 11 lines 38-40).

18. As per claim 28: A clock and data recovery circuit comprising: a first data input receiving a data signal of a first frequency (Cotton fig. 4d-2: input into 150; fig. 6: link data), a clock defining a timing signal (Cotton fig. 4d-1, 4d-2: output from VCXO 100 and into 148) of a second frequency (Cotton does not teach a second frequency but would be obvious as explained below), a phase generator dividing a cycle of the timing signal into a number of N clock phases (Cotton fig. 5a; fig. 6: phase 0-3; fig. 4d-2: divide by 2 in 148); a data sampling component sampling a portion of said data signal (Cotton fig. 4d-2: 150 is sampling input into 150 at the 4 phases) causing a logic output statement based on a truth table (Cotton fig. 8b), said data sampling component comprising a buffer component for buffering said data signal (Cotton fig. 9: D-flip-flops buffer at D input) and a phase detector (Cotton fig. 9: D-flip-flops are detecting phase at their clock input), and a phase selector coupled to said data sampling component, wherein said data signal is buffered by a first, a second and a third group of bistable multivibrators (Cotton fig. 6: flip-flops are buffering), triggered by a first clock phase i, a second clock phase j, and a third clock phase k, respectively, resulting in a buffering of the state of said data signal at said clock phases i, j, and k (Cotton fig. 6: flip-flops are buffering and are triggered by different clock phases).

19. What Cotton does not teach is that the timing signal is of a second frequency. It is common knowledge, based on the Nyquist criteria, that the sampling signal has to be at least

twice as fast as the data signal in order to avoid aliasing. Thus, it would have been obvious to one skilled in the art at the time of the invention to modify Cotton to arrive at the timing signal of a second frequency as recited by the instant claims, because Cotton suggests sampling correctly, and this means that aliasing should be avoided by having a sample timing be at least twice the data rate, in the analogous art of data sampling.

20. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cotton in view of Stuart 3,746,800. Here is how the references teach the claim:

21. As per claim 27: A clock and data recovery circuit as claimed in claim 19, further comprising dual rail amplifiers (not in Cotton but would be obvious). What Stuart teaches is dual rail amplifiers (Stuart fig. 7: flip flops 18, 20, 22, 24, 26, 28). It would have been obvious to one skilled in the art at the time of the invention to modify Cotton with the dual rail amplifiers in Stuart. One would be motivated to do so in order to control clock timing as taught by Stuart.

Allowable Subject Matter

22. Claims 1-5, 8-12, 16-17 are allowed.

23. Claims 14 and 23 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (571) 272-3011. The examiner can normally be reached on Mon, Tues, Thurs and Fri after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PK